Programming margin enlargement by material engineering for multilevel storage in phase-change memory

You Yin,[a] Tomoyuki Noguchi, Hiroki Ohno, and Sumio Hosaka
Department of Production Science and Technology, Gunma University, 1-5-1 Tenjin, Kiryu, Gunma 376-8515, Japan

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In this work, we investigate the effect of the material engineering on programming margin in the double-layered phase-change memory, which is the most important parameter for the stability of multilevel storage. Compared with the TiN/SbTeN cell, the TiSiN/GeSbTe double-layered cell exhibits the resistance ratio of the highest to lowest resistance levels up to two to three orders of magnitude, indicating much larger programming margin and thus higher stability and/or more available levels. Our calculation results show that the resistivities of the top heating layer and the phase-change layer have a significant effect on the programming margin. © *2009 American Institute of Physics*. [doi:10.1063/1.3240408]

Recently, more and more information is required to be stored and treated fast and thus there is a growing need for high-speed and high-density nonvolatile memory (NVM).[1–3] Flash memory, the current mainstream NVM, may not continue to scale due to pressing reliability concerns and geometrical limitations few years later.[2,3] In order to overcome these technical issues, some prospective memories such as nanocrystal memory,[4] ferroelectric memory,[5] magnetoresistive memory,[6] phase-change (PC) memory (PRAM, or PCM),[7–9] resistive memory (RRAM),[10–12] and atomic switch[13] were proposed and attracted much attention in the world in recent years.

PCM has been widely regarded as the post-flash memory due to its almost perfect characteristics.[14–16] It is also very promising for multilevel storage (MLS) because PC between amorphous and crystalline results in a huge electrical resistivity difference up to five to six orders of magnitude, compared with the reflectivity change up to 30%.[17,18] In theory, lots of resistance levels in PCM can be created by controlling crystallinity and/or volume ratio of amorphous to crystalline phases between electrodes.[1,16,19]

However, practical sharp resistance changes[1,20–22] with programming current or voltage in most of the PCM memory cells imply extreme difficulty in controlling crystallinity or volume ratio for MLS. Many techniques such as multichalcogenide-layer structure[9,16,23] and write strategy[24] were proposed to improve the controllability and 4 bit storages were demonstrated 2 years ago. The number of available resistance levels in multilayer structure is limited severely to the number of the chalcogenide layers and MLS of more than four levels has not yet been demonstrated. Write strategy may make many levels more precise but also imply that lots of effort is necessary.

In order to make MLS of more than four levels possible and simplify the programming strategy, we proposed a PCM with a simple double-layered structure. Also TiN/SbTeN (TN/STN) PCM cells exhibited the possibility of ultra-MLS up to 16 resistance levels.[14] The resistance ratio ($R_{highest}/R_{lowest}$) of the highest to lowest levels was only around one order of magnitude, implying very narrow programming margin.

In this letter, we report material engineering in the double-layered PCM for MLS by comparing the TiSiN/$Ge_2Sb_2Te_5$ (TSN/GST) with the TN/STN cells. The resistance ratio ($R_{highest}/R_{lowest}$) in the former cell is demonstrated to be increased to two to three orders of magnitude, implying much larger programming margin and/or higher stability of MLS.

The GST, STN, TSN, and TN layers were deposited using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a background pressure below 5×10^{-5} Pa and a sputtering pressure of 0.2 Pa. N_2 and Ar gases were simultaneously introduced into the chamber during sputtering. For the STN film, gas flow rates of N_2 and Ar are 1 and 14 SCCM (SCCM denotes cubic centimeter per minute at STP), respectively. Current-voltage (*I-V*) characteristics of the devices were measured by semiconductor parameter analyzer (4155B, Agilent Technologies, Ltd.). Device resistance *R* was read out at a low current (e.g., 20 μA). A waveform generator (Model 2571, Tabor Electronics, Ltd.) was adopted to apply single pulses to the devices.

The concept of our proposed double-layered cell can be described based on Fig. 1. Two layers of amorphous PC (*a*-PC) and top heater are deposited above the two electrodes (LEC and REC). Also the dimensions of the cell are labeled in Fig. 1(a). The top heater layer makes it possible that the current path changes from the chalcogenide to the heater. By applying a current higher than the threshold current (corresponding to the threshold voltage[15]), the chalcogenide regions above electrodes switched to crystalline phase due to the formation of conductive filaments and crystallization,[15] as shown in Fig. 1(b). Correspondingly, the cell resistance drops from the initial resistance R_0 to the resistance R_1 with the first crystallization process. Applying increasing current to the cell results in the gradual crystallization (i.e., reduction in the total crystallinity between electrodes) by Joule heating, as shown in Fig. 1(c). This sequent crystallization implies that the cell resistance can be controlled to gradually decrease with programming current.

Figure 2 shows the programming of the TN/STN cell by the current sweepings from 0 to the programming currents I_p.

[a]Electronic mail: yinyou@el.gunma-u.ac.jp.

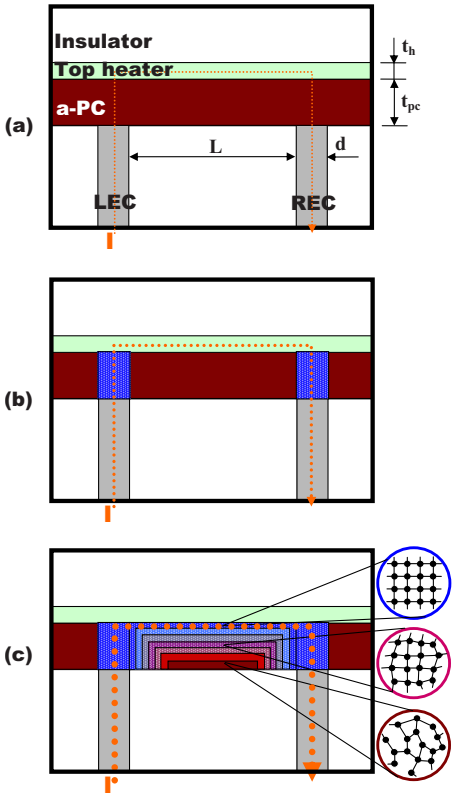

FIG. 1. (Color online) Concept of MLS in the double-layered cell. (a) Highest resistance level R_0 at the initial completely amorphous state. (b) Intermediate resistance level R_1 after the first crystallization via the filament formation and subsequent Joule heating. (c) Intermediate resistance level R_i after crystallization gradually processes by Joule heating.

The programming currents were 0.5, 1, 2, and 3.5 mA. The inset of Fig. 2 shows the sweeping *I-V* curves. It can be seen that the cell resistance can drop gradually with programming current. The initial resistance R_0 was 27.9 kΩ and dropped to around 19.8 kΩ after applying programming current of 0.5 mA. The cell resistance reduced gradually with increasing programming current and it finally dropped to 3.9 kΩ after applying I_p of 3.5 mA. The programming characteristics show that the ratio ($R_{\text{highest}}/R_{\text{lowest}}$) is 7.2, lower than one order of magnitude, allowing very narrow programming margin for MLS. Resistance change with programming current of TSN/GST cell is shown in Fig. 3. It can be seen that the cell resistance dropped by more than two orders of magnitude from the initial resistance of 340 kΩ to the final resistance of 2.3 kΩ, allowing much larger programming margin.

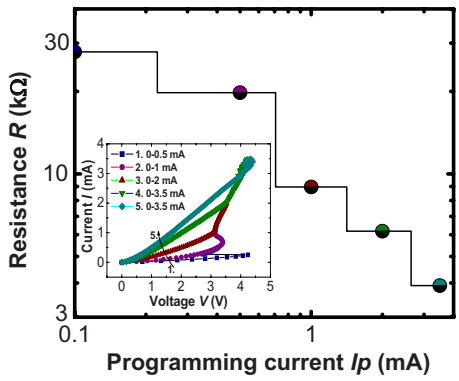

FIG. 2. (Color online) Typical resistance change as a function of programming current of TiN/SbTeN double-layered cell, showing narrow total programming margin of around one order of magnitude.

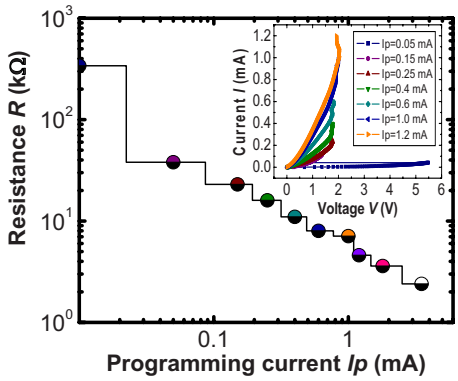

FIG. 3. (Color online) Resistance change as a function of programming current of $TiSiN/Ge_2Sb_2Te_5$ double-layered cell, exhibiting wide total programming margin of more than two orders of magnitude.

Here, the reason why the programming margin can be significantly enlarged by material engineering is considered as follows. Figure 4 shows the programmable resistance ratio with the resistivity ratio (ρ_a/ρ_c) of amorphous to crystalline phases of chalcogenides according to our calculation. In the calculation, the gap length L between electrodes (LEC and REC) and the size d of electrodes shown in Fig. 1(a) are taken to be 400 and 100 nm, respectively. Also the thicknesses of the bottom chalcogenide and the top heater are 80 and 40 nm, respectively. The resistances of the regions above electrodes, which are shown as the dotted blue regions in Fig. 1(b), are both r_1. The resistance of the chalcogenide region between blue regions is r_2. Also the resistances are described as r_{1a}, r_{2a} and r_{1c}, r_{2c} when the corresponding regions are amorphous and crystalline, respectively. The top heater has a resistance of r_h. The resistvities of the amorphous, crystalline chalcogenide and heating layer are ρ_a, ρ_c, ρ_h, respectively. To simplify the calculation, the total circuit resistance, excluding that of double layer, is neglected first. Also if $\rho_a \geq \rho_h \geq \rho_c$ is reasonably taken into account, the cell resistance can be calculated as follows. The initial cell resistance R_0 (R_{highest}) can be expressed as

$$R_0 \approx 2r_{1a} + r_h = 1.6 \times 10^7\ [m^{-1}]\rho_a + 10^8\ [m^{-1}]\rho_h. \quad (1)$$

And the resistance R_1 after initial crystallization as shown in Fig. 1(b) can be described as

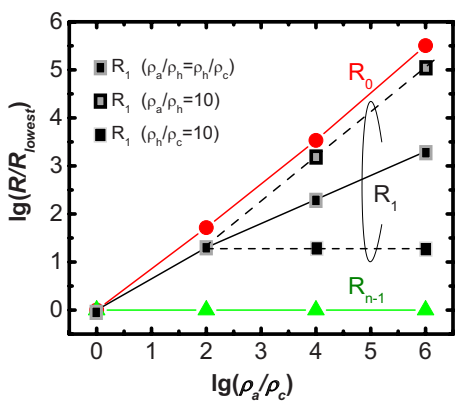

FIG. 4. (Color online) The effect of material characteristics on the programming margin.

$$R_1 \approx 2r_{1c} + r_h = 1.6 \times 10^7 \ [m^{-1}]\rho_c + 10^8 \ [m^{-1}]\rho_h. \quad (2)$$

The final lowest resistance R_{n-1} (or R_{lowest}) after complete crystallization can be expressed as

$$R_{n-1} \approx r_{2c} = 5 \times 10^7 \ [m^{-1}]\rho_c. \quad (3)$$

The calculated resistance ratio R_0/R_{n-1} (or $R_{\text{highest}}/R_{\text{lowest}}$) as a function of resistivity ratio can be logarithmically plotted as Fig. 4 according to these three equations. It can be seen that the resistance ratio R_0/R_{n-1} increases with the resistivity (ρ_a/ρ_c). From our previous description, it can be known that the intermediate resistance levels cannot be created between the initial resistance R_0 and the resistance R_1 after the first crystallization via filament formation by electric field and subsequent Joule heating. So it is necessary to find optimized conditions to effectively enlarge the practically programmable margin by material engineering. Three resistivity conditions are taken into account here, (a) $\rho_a/\rho_h = \rho_h/\rho_c$, (b) $\rho_a/\rho_h = 10$, and (c) $\rho_h/\rho_c = 10$. Condition (a) means that the resistivity of heating layer is logarithmically located in the middle of those of amorphous and crystalline chalcogenide phases. The calculated results imply that the relatively high resistivity ρ_h can effectively increase the programmable margin R_1/R_{n-1}.

Let us consider the programming characteristics of TSN/GST and TN/STN double layer cells described above. The resistivity ratio (ρ_a/ρ_c) of STN, around three to four orders of magnitude is lower than that of GST, five to six orders of magnitude, which should be the main reason why the TSN/GST has much larger resistance ratio R_0/R_{n-1}. The total circuit resistance, neglected in our above calculation, can raise the final resistance level and thus practically reduce the programming ratio R_0/R_{n-1}.

In conclusion, we have investigated the material engineering on the programming margin for MLS. The $TiSiN/Ge_2Sb_2Te_5$ cell was demonstrated to have a large programming margin mainly due to the large resistivity ratio of amorphous to crystalline phases of chalcogenide $Ge_2Sb_2Te_5$ material. The resistivity of heating layer compared with those of the chalogenide material can have a great effect on the programmable resistance margin.

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