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Recrystallization process controlled by staircase pulse in phase change memory

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ABSTRACT

In this study, we investigate the recrystallization process in phase-change memory by applying staircase pulses. The controlled recrystallization process is expected to be applied to freely achievable multilevel storage. Simulation results exhibit that the phase change material is heated above its melting point during the first subpulse of the staircase pulse and then annealing temperature can be controlled by varying amplitude of the second subpulse. This implies that the recrystallization region is controllable by applying staircase pulses. V-shaped resistance change vs. the amplitude of the second subpulse, which is caused by the growth and the shrinkage of recrystallized region, is obtained at each width of second subpulse.

1. Introduction

There is an increasing demand for next-generation memory characterized by fast speed, high density, nonvolatility and low-power consumption [1]. Recently, some prospective memories with these characters such as nanocrystal memory [2], ferroelectric memory (FeRAM) [3], magnetoresistive memory (MRAM) [4], phase-change memory (PRAM, or PCM) [5–7], resistive memory (RRAM) [8–9] and atomic switch [10] were proposed and widely researched to overcome the disadvantages of current mainstream flash memory.

PCM has attracted much attention all over the world and has been regarded as post flash memory because of its excellent performances in these promising memory technologies [1]. PCM is based on the huge resistance change caused by fast and reversible amorphous-crystalline phase transition [11–13]. It is demonstrated that lateral PCMs have many advantages such as low power consumption due to the small heat loss into the underlying substrate, compared with conventional vertical PCMs [1,13–14]. In order to further increase storage capacity in lateral PCM device, it was discovered by our group that 16 distinguishable resistance levels can be readily created by gradually increasing the total crystallinity, programmed by current sweeping [15,16].

However, the transition among these multiple levels in the lateral cell is yet a big technical problem for application although ultramultiple level storage was easily realized in our proposed lateral double-layered memory cell. The multilevel storage was demonstrated by application of increasing currents for gradual crystallization from the as-deposited amorphous state. This programming method showed great difficulty in switching back to the programmed resistance level from low-resistance crystallized level by simply applying currents. And it is difficult to develop a fast constant current pulse generator for the practical application using this sweeping method. Therefore, it is necessary to develop some new programming technologies for freely-achievable state transition. In other words, the operation for these transitions does not rely on the previous state. In this work, the simplest staircase-like modulated signal voltage pulse was adopted. Here, we report the effect of the staircase-like pulse with two subpulses on the recrystallization control in the lateral double-layered phase-change memory for freely-achievable-multilevel storage.

2. Concept of crystallization control

The concept of staircase pulse controlled recrystallization for freely achievable multilevel storage is schematically illustrated as shown in Fig. 1. A high resistance level with a low crystallinity can be switched to a low resistance level by increasing the total crystallinity in the device. These easy transitions via our previous current-sweep programming are shown as black arrows between any two neighboring resistance levels, starting with the high-resistance amorphous state R_a. These transitions are dependent on the previous resistance state. For example, the resistance level R_2 can drop to the lower resistance level R_c with our previous current-sweep programming. However, for a practical memory, it is certainly expected that the resistance level can reach freely to any other level as shown in Fig. 1(a). To realize a fast overwrite multi-

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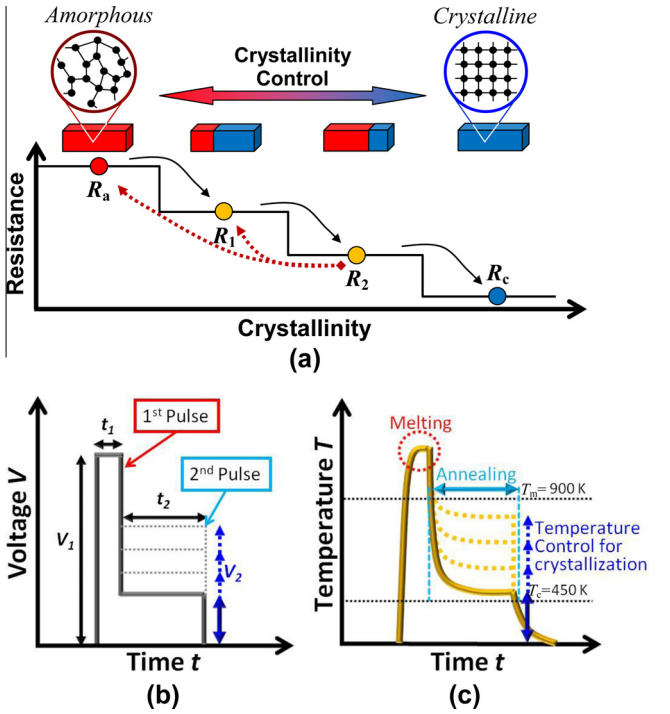

Fig. 1. Concept of recrystallization control by applying a staircase pulse. (a) Resistance changes with crystallinity. (b) The staircase pulse which is composed of a high but short first pulse for melting to initialize the storage state and a long but low second pulse to control the annealing temperature. (c) The temperature changes after the application of staircase pulse.

level storage memory, for instance, R_2 must reach not only to the lower resistance level (R_c) with a higher crystallinity but also to any other higher resistance levels ($R_a, \ldots, R_1$) with lower crystallinities. These transitions are shown as the red dotted arrows.

The detailed approach to crystallinity control for freely achievable multilevel storage in this study can be further explained with programming methods in Fig. 1(b and c). In the conventional operation of a PCM device, only simple electrical pulses are applied to switch between amorphous and crystalline phases. A high and short electrical pulse heats the phase-change material above its melting point (T_m) and then cools it down suddenly, resulting in a completely amorphous phase with the lowest crystallinity. On the other hand, an intermediate and long electrical pulse heats the phase-change material between its melting point and crystallization temperature (T_c) and maintains that temperature for a certain period, leading to the completely crystalline phase with the highest crystallinity.

Here, we proposed a staircase-shaped pulse, as shown in Fig. 1(b), to first heat the phase-change material above T_m and then allow it to cool and maintain a temperature between T_m and T_c for a certain annealing period of t_c, as shown in Fig. 1(c). The staircase-shaped pulse is composed of two subpulses for amorphization and subsequent control in recrystallization. The first amorphization subpulse with an amplitude of V_1 and a pulse width of t_1 is used for amorphizing the phase-change material to reset its previous state to amorphous. This subpulse makes the operation for the transition to any resistance level independent on the previous state. And the second crystallinity-control subpulse with an amplitude of V_2 and pulse width of t_2 is used for controlling the total crystallinity (recrystallization region) from completely amorphous to completely crystalline phases, as shown in Fig. 1(b). The two parameters of V_2 and t_2 of the second subpulse are of great importance for the control of recrystallization via the annealing temperature and time. Here, we mainly discuss the effect of the amplitude V_2 of the second subpulse on the total crystallinity for freely achievable multilevel storage.

3. Simulation results

Fig. 2 shows the schematic structure used in simulation. The active layers of the device consist of a 150-nm-thick $Ge_2Sb_2Te_5$ (GST) layer and a 50-nm-thick $TiSi_3$ layer. Most widely researched GST is adopted here as phase change material. Two underlying TiN electrodes connects the defined GST film.

Highest temperature change in GST layer was summarized when staircase pulse is applied to two TiN electrodes. Fig. 3 shows the highest temperature change with time simulated using a commercially available finite-element analysis software COMSOL 4.1. The curve (a) shows the temperature profile induced by a simple pulse ($t_2 = 0$) of 8 V, 50 ns. The temperature distribution at 50 ns is shown in the inset figure of Fig. 3(A). The region between electrodes is heated above the melting point T_m (around 900 K for the GST film [17]). The quench time from its melting point to its crystallization temperature T_c (around 450 K for the GST film [18–19]) is about 15 ns, which is short enough to keep the atoms in the highly disordered state and be amorphized [1]. Then the annealing temperature can be controlled by applying a staircase pulse with a 8 V, 50 ns first subpulse and 100 ns second subpulse with an amplitude of 0–6.4 V. Typical temperature distributions for pulses with second subpulse amplitudes of 3.2, 4.0, 4.8, and 5.6 V are shown in Fig. 3(B–D), and, respectively. It is obvious that the recrystallization region increases with second subpulse amplitude. This means that the recrystallization region can be controlled simply by the amplitude of the second subpulse. As is well known for the phase change materials, the higher the annealing tempera-

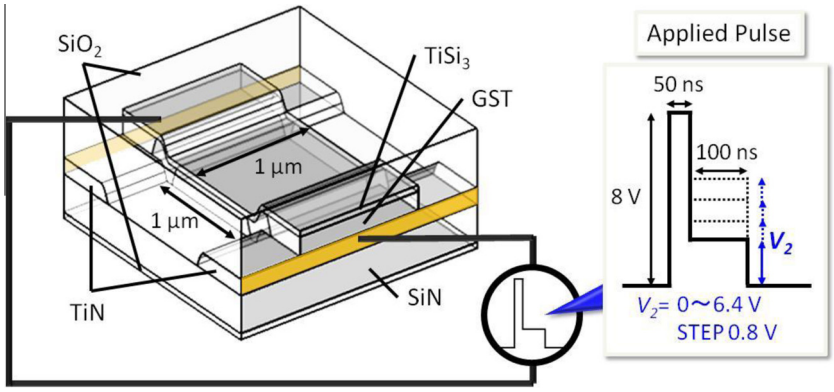

Fig. 2. Three dimensional model for finite elemental analysis.

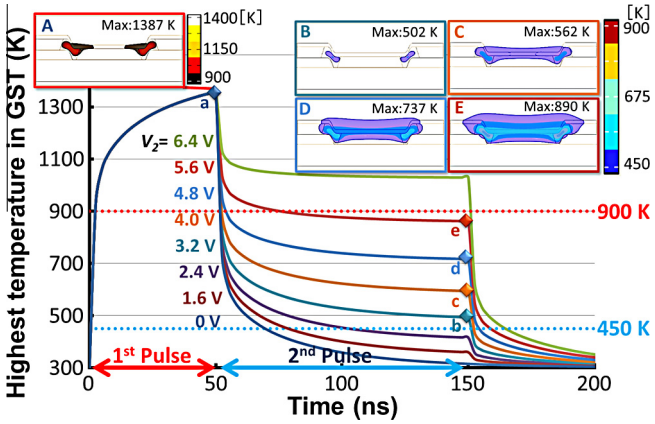

Fig. 3. Simulation results of highest temperature profile.

ture for a certain annealing time, the higher the crystallinity [19–20]. The high crystallinity corresponds to a low device resistance for a memory device so the device resistance can be controlled by the applied staircase pulse.

4. Experimental results and discussion

The images of the fabricated devices are shown in Fig. 4. The GST and $TiSi_3$ layers were deposited using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a background pressure below 5×10^{-5} Pa and a sputtering pressure of 0.2 Pa. The measurement system consisted of pulse application and resistance measurement controlled by LabVIEW, as shown in Fig. 5. A waveform generator (Model 2571, Tabor Electronics, Ltd.) was adopted to apply staircase pulses to the devices. Device resistance R was read out at a low voltage.

The experimental results on the recrystallization control are shown in Fig. 6. The staircase pulses with a first subpulse of 8 V, 50 ns and a second subpulse of 0–5.6 V was applied to the device. The width of the second subpulse is 50, 100 and 500 ns. The device resistance changed by more than one order of magnitude owing to the large recrystallization region when the wide 500 ns second subpulse was applied. The resistance change looks like a letter of "V" instead of "U", which is typical for the device resistance change programmed by conventional pulses [21–22]. This gradual change in resistance is very useful for the application to multilevel storage because of many available intermediate resistance levels [15–16,23].

The device resistance changed a little at a small pulse amplitude V_2 of 1.4 V because the recrystallization started to occur between the two electrodes. At this voltage, the applied pulse induced a temperature profile as shown in the middle inset in a small region. In other regions, the temperature profile would be like the left inset. As a result, the heating at a temperature between crystallization temperature and melting point took place in a small region and resulted in a partial recrystallization, accompanying a small resistance drop. The resistance further decreased until 2.1 V when the recrystallization region became larger. The resistance almost did not change even after a pulse with a subpulse amplitude of 2.4 V. At this voltage range from 2.1 to 2.4 V, the applied pulse induced a temperature profile as shown in the middle inset in the region between electrodes. In other words, the heating temperature fell in the range between crystallization temperature and melting point. It is thus thought that the region between electrodes almost became fully crystallized. The device resistance increased again from 2.6 V, which was caused by the decreased recrystallization region. At this voltage, the applied pulse induced a temperature profile as shown in the right inset in a small region. In other regions,

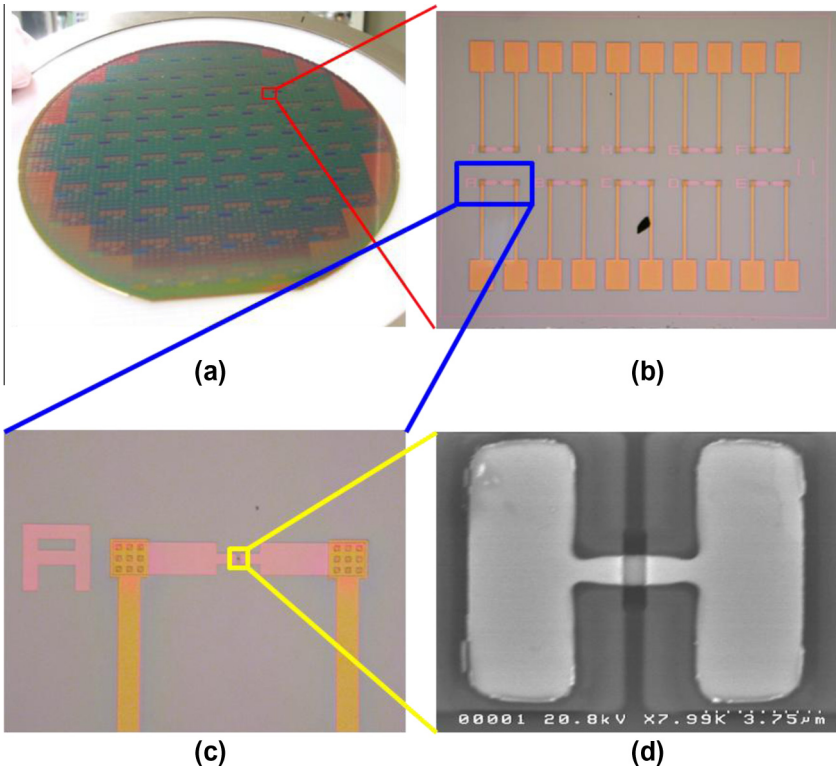

Fig. 4. (a) Optical image of wafer where chips are integrated. (b) Optical image of one chip where 10 devices are integrated. (c) Optical image of a device. (d) Scanning electron microscopy image of the central part of a device.

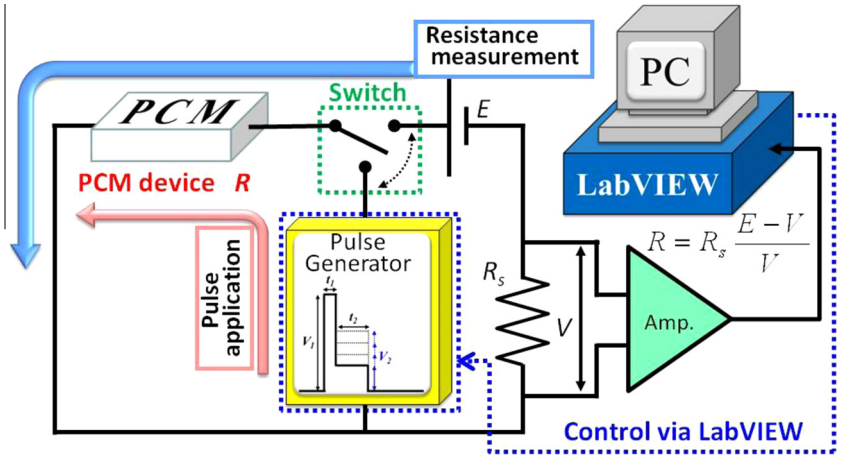

Fig. 5. Circuit for device programming and measurement.

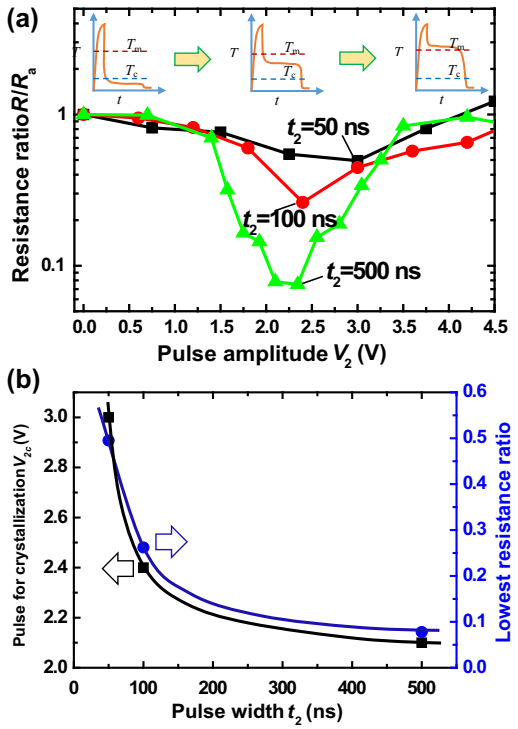

Fig. 6. (a) Resistance change vs. the amplitude of the second subpulse. (b) Pulse for crystallization and lowest resistance ratio as a function of the width of the second subpulse.

the temperature profile would be like the middle inset. As a result, the heating at a temperature higher than the melting point took place in the small region and resulted in a partial amorphization, accompanying a small resistance increase. Finally, the device resistance returned to the high resistance level corresponding to the completely amorphous state.

It should be noted that the resistance level at a voltage lower than about 1.0 V was the same as that at a voltage higher than about 3.5 V. Phase change material could not be recrystallized due to its low heating temperature ($<T_c$) at a low second subpulse voltage after melting at a high first subpulse as shown in the left temperature profile inset in Fig. 6(a). In this case, the phase change material was in amorphous state and correspondingly the device had a high resistance level. And phase change material could not either be recrystallized due to its high heating temperature ($>T_m$) at a low second subpulse voltage after melting at a high first subpulse as shown in the right temperature profile inset in Fig. 6(a). In this case, the device also had a resistance level since the phase change material was in amorphous state.

The device resistance R decreased only to about $0.25R_a$ when the wide 100 ns second subpulse was applied. For the short 50 ns second subpulse, the device resistance dropped only a little with increasing pulse amplitude. This little change in device resistance should be due to the very small recrystallization region induced by the pulse with the short 50 ns second subpulse. The pulse amplitude for crystallization as a function of pulse width, derived from the Fig. 6(a), is shown in Fig. 6(b). As we can see, the pulse amplitude for recrystallization decreased with the pulse width, which is in consistent with the required energy for recrystallization. The lowest resistance ratio as a function of pulse width is plotted in Fig. 6(b). The lowest resistance ratio of R/R_a for the pulse width of 50 ns was as high as 0.5. This means that the recrystallization region induced by the pulse was almost not proceeded even after the phase change material melted. The lowest resistance for the pulse width of 100 ns decreased to about 0.25, implying the promoted recrystallization in the device. It further decreased to about 0.08 for the pulse width of 500 ns. Recrystallization region became large enough to enable the resistance decrease by more than one order of magnitude.

It was believed that the programming by the staircase pulses opens the way to recrystallization control for freely-achievable-multilevel storage. Varied pulses with different pulse widths of second subpulses can also be expected to control the crystallinity for freely-achievable-multilevel storage. The resistance drift and the crystallization of the amorphous phase during programming might have an influence on the reliability but this can be well improved by adopting write strategies. In the future, we expect that recrystallization control for fast freely-achievable-multilevel storage can be realized by applying staircase pulses with both optimized pulse amplitudes and pulse widths of second subpulses.

5. Conclusions

The staircase pulse with two subpulses was proposed for programming the phase-change memory for freely-achievable multilevel storage. The second subpulse is critical to control the total crystallinity based on our simulation results. And experimental results showed that the device resistance gradually decreased and then increased with increasing the amplitude of second subpulse during the enlargement and shrinkage of recrystallization region. This staircase pulse programming technique exhibited the possibility that any resistance levels are freely achieved.

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