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Controlled promotion of crystallization for application to multilevel phase-change memory

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In this work, controlled promotion of crystallization was investigated for application to multilevel storage by using a vertical $TiSi_3/Ge_2Sb_2Te_5/TiN$ cell with a thin phase-change layer. Finite element analysis exhibits that crystallization gradually proceeds with increasing applied current in the radial direction after a filament forms. Current-voltage (*I-V*) characteristics show that the device resistance corresponding to the crystallized area drops with increasing sweeping current. Eight resistance levels are demonstrated and their effective crystalline thicknesses are estimated from fitting of *I-V* curves in the subthreshold regime on the basis of the trap-limited model. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4730439]

Large-capacity nonvolatile memory is increasingly demanded as the portable electric equipments such as the note computer, smart phone, and so on are widely used in our daily life.[1–9] Multilevel storage (MLS), data storage of more than two levels per memory cell, has attracted much attention in recent years because it is thought as the most promising method to increase capacity with low cost. The possibility of MLS was demonstrated in both conventional flash memory and emerging memories in the last decade.[10–16]

Several intermediate resistance levels in phase-change memory (PCM) are available by carefully controlling the phase-transformation of chalcogenide in theory. Distinct and stable intermediate resistance levels, which were obtained by controllable layer-by-layer crystallization or amorphization, were demonstrated by using a multilayer structure.[17,18] However, the number of available resistance levels N_R is strictly dependent on the number of the layers of phase-change chalcogenide N_{PC} for MLS based on multilayer structure. A relationship between N_R and N_{PC} can be simply described as $N_R = N_{PC} + 1$. There is no report of MLS of eight levels corresponding to three bit by using multilayer structure since seven layers of chalcogenide become required. It would be a serious technical issue to make so many layers of chalcogenide sequentially crystallize or amorphize layer by layer. And it would also be a hard work to have enough programming margins when such a seven-layer MLS cell is designed based on material engineering. MLS with more than eight resistance levels was demonstrated by some groups based on programming algorithm.[19,20] However, it is necessary to take much time to make the programmed resistance fall into the range of the wanted level by confirmation and rewriting. On the other hand, it is based on amorphization process characterized by high power consumption, and the mechanism was thought to be a serial volume change of amorphized area when a device structure with a low ratio (*d/t*) of the diameter of contact hole *d* to the thickness of chalcogenide *t* was adopted.

In this Letter, we report the controllability of crystallization characterized by low power consumption in the vertical PCM with a high ratio *d/t*, which is gradually promoted in parallel on the basis of finite element analysis.

Cross section of our device is schematically shown in Fig. 1. 50-nm-thick TiN was deposited on $SiN/SiO_2/Si$ substrate as the bottom electrode. The SiO_2 hole was fabricated by wet etching. The depth of the hole is 175 nm. And the bottom size of the contact hole is 700 nm. 50-nm-thick $Ge_2Sb_2Te_5$ (GST) film as the phase change layer and $TiSi_3$ as the top electrode were deposited using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a background pressure below 5×10^{-5} Pa, a sputtering pressure of 0.2 Pa, and a radio frequency power of 100 W. Current-voltage (*I-V*) characteristics of the device samples were measured by semiconductor parameter analyzer (4155B, Agilent Technologies, Ltd.).

The crystallization (C-GST) promoted with increasing amplitude of programming currents in our device was investigated on the basis of finite element analysis. The device begins with a fully amorphous GST (A-GST). The first crystallization (or filament formation) is induced by an electric field, which is higher than a certain value (threshold electric field[21,22]) when a current of 0.5 mA was applied. The corresponding outline of crystallized area (α) is shown in Fig. 2(a). Crystallization induced by Joule heating is promoted by applying a higher current 0.8 mA, and the outline becomes the curve of β. Similarly, the outline of crystallized area changes from χ to δ, ε, φ, and finally to γ with further increasing current from 1.2 to 1.8, 2.5, 3.5, and then 5.0 mA, respectively. Fig. 2(b) shows the simulation result of crystallization promotion in GST layer when 1.8-mA current is applied. The outline of crystallized area of GST was the curve of χ. The temperature distribution in GST when 1.8-mA current is applied was simulated using finite element method. Contour curves of 750, 650, 550, and 450 K are shown in the figure. Here, we set the crystallization temperature of GST as 450 K. And thus, it can be easy to understand that outline of crystallized area of GST changes from the curve of χ to δ after 1.8-mA current is applied.

Fig. 3 shows *I-V* characteristics of our device when current was swept from 0 to programming current and then backward to 0 mA. As we can see, there was no change after
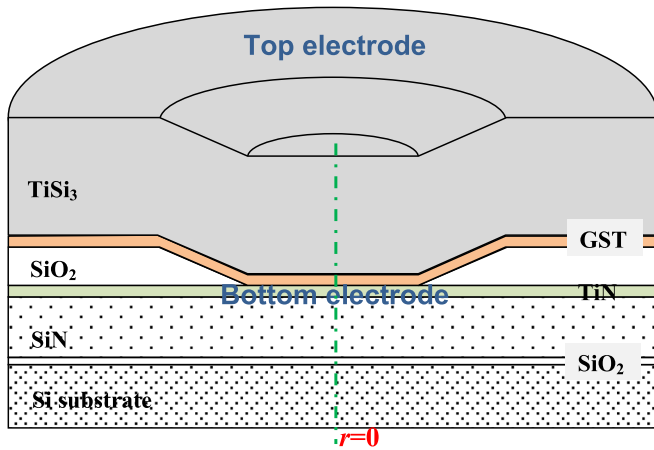
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FIG. 1. Diagram of the phase-change memory cell with a TiSi$_3$/Ge$_2$Sb$_2$Te$_5$/TiN vertical structure.

the first current sweeping of S1 (0–0.4–0 mA). However, the second sweeping of S2 (0–0.5–0 mA) resulted in a distinct difference between the forward and the backward curves. Especially, a sudden change due to filament formation[21,22] was observed. The forward part *I-V* curve in the range of
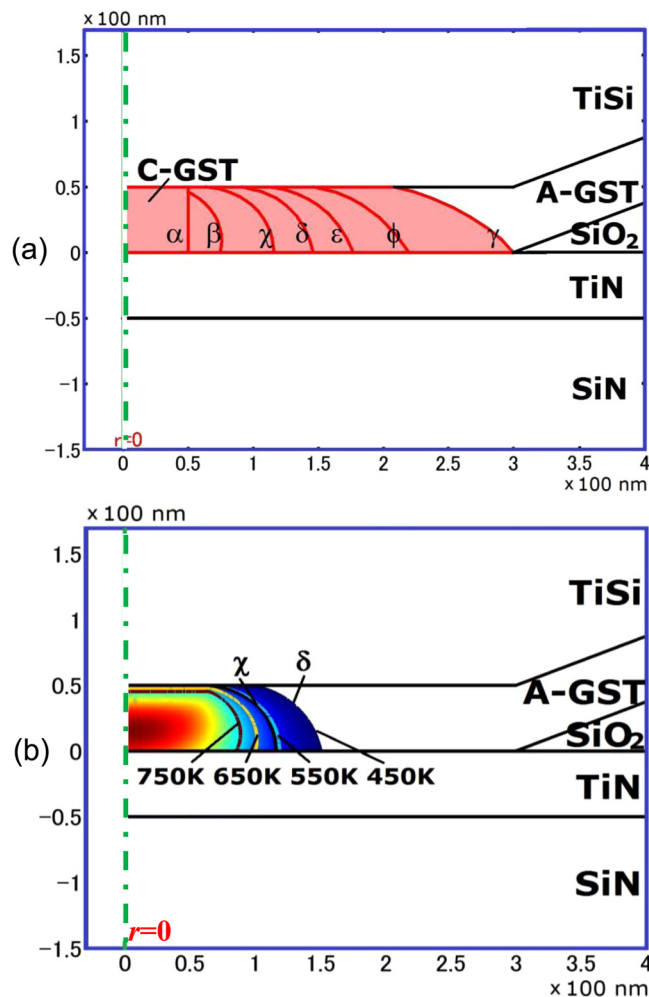

FIG. 2. (a) Simulated crystallization promotion based on finite element analysis. Crystallization begins with a filament formation with an outline of α. Crystallization then proceeds from β to χ, δ, ε, φ, and finally to γ. (b) Temperature distribution of GST when a 1.8 mA pulse is applied. The outline of crystallized area changes from χ to δ.
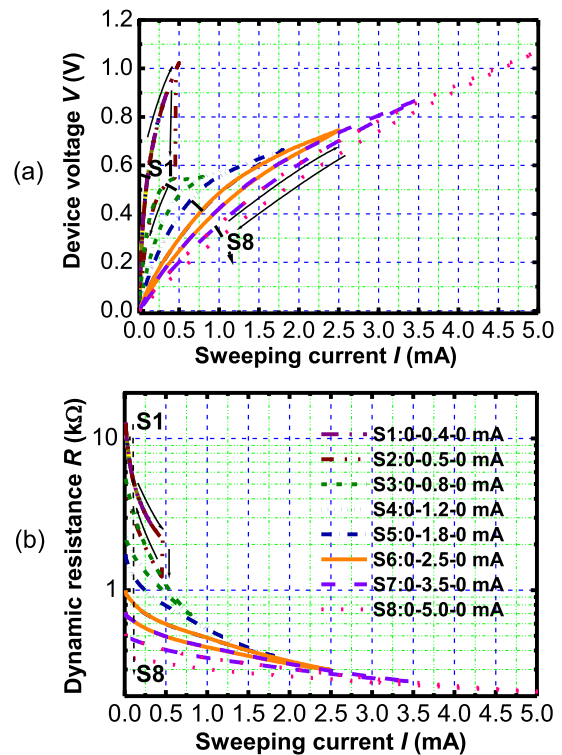

FIG. 3. (a) *I-V* curves obtained by current sweeping. (b) Dynamic resistance change as a function of sweeping current.

0–0.5 mA during the third sweeping of S3 (0–0.8–0 mA) perfectly overlapped the backward part (0.5–0 mA) of S2. This implies the stability of the programmed resistance level. Further increasing current from 0.5 to 0.8 mA almost did not change the voltage across the device. And it is very clear that there exists a difference between the backward and forward parts. Similar phenomenon can be observed for all the other sweepings of S4, S5, S6, S7, and S8. Fig. 3(b) shows the dynamic resistance ($R = V/I$) as a function of the sweeping current. The resistance suddenly dropped at a current of around 0.45 mA. And the programmed resistance level remained when sweeping backward to 0 mA. It is very interesting that the programmed resistance level did not change when current was swept in the range of 0–0.5 mA again. This proved that the programmed resistance level was stable. The resistance further dropped once a higher current was swept in the range of 0.5–0.8 mA. The backward dynamic resistance was very different from the forward, which means that the resistance level had been changed during the current sweeping of 0.5–0.8 mA. The device resistance levels were programmed in the same way at higher currents.

I-V curves of eight resistance levels are shown in Fig. 4(a). The symbol represents the experimental data, and the line represents the fitting, which is based on the trap-limited transport model of Ielmini and Zhang.[23] In the earlier literature,[24] Hill investigated the nature of the electrical conduction process in amorphous solids, using as a basis the ionization of local defects by an applied field, and described the exponential field dependences without associating them with any hopping. The model of Ielmini and Zhang, which is adopted here, describes the electrical transport of an amorphous chalcogenide at the subthreshold conduction regime through a thermally assisted hopping for conduction through
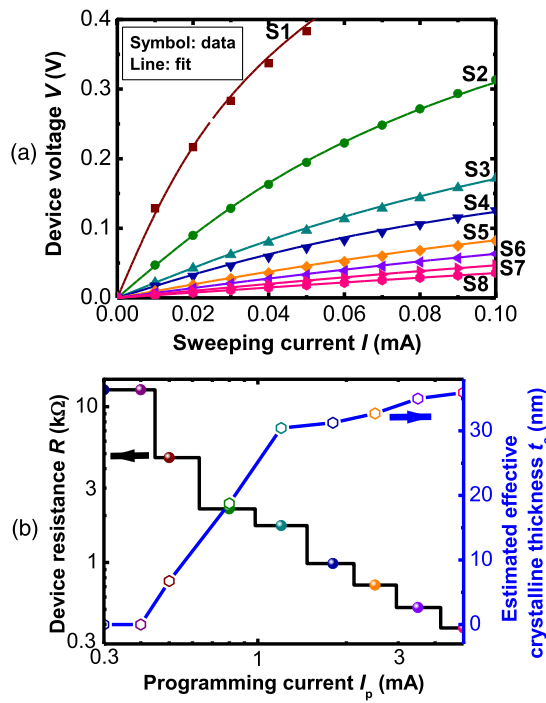
FIG. 4. (a) Measured and fitted I-V curves in the subthreshold regime. (b) Device resistance levels and corresponding estimated effective crystalline thicknesses as a function of programming current.

localized states.[23,25,26] The nonlinear relationship between device current I and device voltage V can be expressed as the following analytical model:

$$I = \frac{1}{R_0 \beta} \sinh(V\beta), \qquad (1)$$

where β is the subthreshold slope (STS) and R_0 is the low-field resistance. And the subthreshold slope β is defined as

$$\beta = \frac{q}{kT} \frac{\Delta z}{2(t_a - u_c)}, \qquad (2)$$

where q is the elementary charge, Δz is the average distance between traps, k is the Boltzmann constant, T is the temperature, u_c is the effective thickness of crystalline GST, and t_a is the thickness of GST, which is initially in amorphous state. As we can see, the fitted I-V curves are in good agreement with the experimental data. The derived effective crystalline thickness is summarized in Fig. 4(b). The device resistance readout at a very low current as a function of programming current is also shown in Fig. 4(b). The device resistance was 12.8 kΩ initially in amorphous state and did not change at 0.4 mA at all. The resistance dropped to 4.7 kΩ at a programming current of 0.5 mA. Then, a higher programming current caused a resistance drop to 2.2 kΩ at a programming current of 0.8 mA. The resistance further dropped to 1.7 kΩ by increasing the programming current to 1.2 mA. Similarly, the increasing programming current induced a decreased resistance level. The device resistance reduced to 0.38 kΩ after applying a programming current of 5 mA. Let us take a look at the estimated effective crystalline thickness t_c as a function of programming current I_p again. The estimated effective crystalline thickness was 0 nm at currents of 0.3 and 0.4 mA. It increased very fast until 1.2 mA was applied. After

that, it increased at a very low speed. This can be also understood from the crystallization promotion based on finite element analysis. The crystallization promotion in the central area including filament formation and crystallization enlargement from α to β and χ of the first stage had a great influence on the increase in effective crystalline thickness. But the crystallization promotions to δ, ε, ϕ, and γ in the peripheral area in the second stage had a little influence on the increase in effective crystalline thickness. Thus, distinct and stable resistance levels were created here, and these levels were induced by current-driven programming. These discrete resistance levels corresponding to different effective crystalline thicknesses were determined by the programming currents. It should be noted that it is possible to obtain a desired number of resistance levels by appropriately changing the number of programming currents.

In summary, we demonstrated that the number of distinguishable resistance levels can reach eight and even higher by current-sweeping. These resistance levels were created from the initial threshold switching and the subsequent controlled promotion of crystallization induced by Joule heating. The resulting resistance levels were relatively stable. The technique enables the ultra-high-density non-volatile memory.

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